FEATURES

- Low power CMOS
- One pulse conversion
- 7 bit resolution
- 10 MHz sampling rate
- TTL & CMOS interface
- Three state outputs
- 20 & 24 pin, 300 mil DIP
- Military & Industrial temp ranges
- Half LSB versions available
- Serveral package options

VERSIONS

USC1070-7 bit, high speed
USC1071-7 bit, for 12 bit 1/2 flash
USC1072-7 bit, ultra low power
USC1073-7 bit, 20 pin package
USC1170-7 bit, 3-state output

DESCRIPTION

The USC1070 is a CMOS flash (parallel) A/D converter designed for sampling at rates up to 10 MHz at very low power operation. The USC1073 utilizes the 1070 die for low cost 7 bit converters in 20 pin plastic packages. The USC1071 uses a modified die for 12 bit half flash applications. The USC1072 die is an ultra low power converter. The USC1170 and 1173 are tri-state output versions of the standard converters.

Conversion is accomplished with only one pulse. Data appears at the outputs following the conversion clock transition. The converter is ready after a minimum reset time. No extra clock steps are required to bring data out.

Underrange and overrange status lines indicate whether the input signal is below or above the input range. The nominal input voltage range is -3.2V to +3.2V and +/-2.5V has been used in many applications.

The family of devices may easily be interfaced to TTL & CMOS logic. The standard converters have open-drain N-channel devices to the digital ground, Vgnd. The 11xx devices have tri-state output drivers to connect directly to a data bus.

Both military and industrial temperature range devices are available. Special test requirements and mill screening (883C) may be ordered. A wide variety of packages are also available. The standard packages are 300 mil 24 pin ceramic, 300 mil 20 pin plastic, 600 mil 24 pin ceramic, and 24 pin Leadless Chip Carriers (LCC) packages. Die are also available for hybrids and other special packaging.

PIN CONFIGURATION

```
   Vgnd  1  20  Vdd
   -Vref  2  19  D1 (LSB)
       BIAS  3  18  D2
       -Vref/2  4  17  D3
          Vin  5  16  D4
       REF Center  6  15  D5
        +Vref/2  7  14  D6
           Vss  8  13  D7 (MSB)
           +Vref  9  12  CLK
     Overrange 10  11  Vgnd
   Vgnd  1  24  Vdd
   Underrange  2  23  D1 (LSB)
       -Vref  3  22  D2
          BIAS  4  21  D3
       -Vref/2  5  20  D4
          Vin  6  19  D5
       REF Center  7  18  D6
        +Vref/2  8  17  D7 (MSB)
           Vss  9  16  NC
           +Vref 10  15  CLK
     Overrange 11  14  Phase
     Vgnd 12  13  CE
```
ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage (Vdd-Vss)
Logic Supply (Vdd-Vgnd)
Logic Output Voltage (Vo-Vgnd)
Logic Input Voltage
Vin Reference Voltages
Idd Supply
Temperature Range
  Storage
  Operating

12V max
7V max
8V max
Vgnd-0.3V, Vdd + 0.3V
Vss min, Vdd max
20mA max

-65°C to + 150°C
-55°C to + 125°C (military)
-25°C to + 85°C (industrial)

ELECTRICAL CHARACTERISTICS

Test Conditions Temp. = + 25°C
Vdd = 5V
Vss = -5V
Vgnd = 0V
Idd = 15mA
+Vref = +3.2V - Vref = -3.2V
Clock = 8 million samples per second (MSPS)
Source Impedance = 100 ohms

COMMON CHARACTERISTICS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Quantizing Error</td>
<td>-1/2</td>
<td>+1/2</td>
<td>LSB</td>
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<tr>
<td>Logic Supply (Vdd-Vgnd)</td>
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<td>6</td>
<td>V</td>
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<td>Analog Inputs:</td>
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<tr>
<td>Full Scale Range (Ref)</td>
<td>Vss + 1.5</td>
<td>Vdd-1.5</td>
<td>V</td>
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<td>pF</td>
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<td>Input Current (DC)</td>
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<td>1000</td>
<td>uA</td>
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<tr>
<td>Input Impedance</td>
<td></td>
<td></td>
<td>MOhm</td>
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<tr>
<td>Digital Inputs:</td>
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<td>Low Voltage (Vil = 0)</td>
<td>1.5</td>
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<td>V</td>
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<tr>
<td>High Voltage (Vih = 1)</td>
<td>3.5</td>
<td>+/-1</td>
<td>V</td>
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<tr>
<td>Input Current</td>
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<td></td>
<td>uA</td>
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<tr>
<td>Logic Outputs:</td>
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<tr>
<td>High Voltage (open drain)</td>
<td>7</td>
<td>4</td>
<td>V</td>
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<tr>
<td>High Voltage (3-state)</td>
<td>.7</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Low Voltage (I0 = 6mA)</td>
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<td></td>
<td>mA</td>
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<tr>
<td>Sink Current (Vo = 0.7V)</td>
<td>25</td>
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<td>nS</td>
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<tr>
<td>Minimum Rest Pulse Width</td>
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<tr>
<td>Max Input Signal Slew Rate</td>
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<td>+/-1</td>
<td>Bits</td>
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<td>Resolution</td>
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<td>Linearity Error</td>
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</table>

TIMING DIAGRAM

PHASE(PIN 14) = HIGH
(Logic 1)¹

CK

RESET
SAMPLE

CE

90nSEC MAX.
20nSEC MAX.
20nSEC MIN.
DATA AVAILABLE

20nSEC MIN.

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*NOTE:
Timing for PHASE = Low (logic 0) is same as above except the CK and CE lines are inverted. Output data is NOT inverted and is independent of the PHASE line. All data output lines are high when CK is in RESET, the chip is disabled (CE + Phase = 0), or the chip is in Overrange. (Underrange condition has no effect on data output pins.)
DEVICE OPERATION

The internal features of the flash converter family consist of a set of reference resistors, 130 voltage comparators, NAND gates, 128 encoders, output buffers, and clock generation circuitry. A reference voltage is applied between + Vref and -Vref driving a resistor with 128 taps. The taps provide the set of voltages to the inverting inputs of the comparators. In the RESET mode the comparator outputs are disabled. When the CLOCK changes, the comparator outputs are latched into their new state. The digital state is determined by the location where the comparators make the transition from all high to all low outputs. This location is encoded into a 7 bit code that is gated to the output terminals.

Three control lines are used: CLOCK, CE (Chip Enable), and PHASE. The PHASE line determines the active state of the CLOCK and CE lines. With a high PHASE line, Vin is sampled on the falling edge of the CLOCK line and CE is active low. The state of CLOCK for a sample and CE is active high for a low PHASE line. The Chip Enable line activates the digital outputs. With the standard devices external resistors will pull the outputs high when disabled. The outputs of the 3—state devices (USC117x) will go to a high impedance state with CE disabled. During the RESET mode of the CLOCK the outputs will be in a high state.

Two status lines are available: OR (OVERRANGE) indicating that Vin is greater than + Vref at the sample and UR (UNDERRANGE) signaling that Vin is less than -Vref. The active state of these two signals is high. The OR and UR signals will be low during RESET mode.

Care should be taken to prevent driving any pin beyond the supply rails. The three control input pins (CLOCK, CE, PHASE), the digital output pins (D1-D7) and the status pins (OR UR) should not be driven below Vgnd (digital ground). Any of these conditions could cause latch up. During initial debug of a circuit using the devices, one should use a 10 ohm resistor in series with the Vdd (+5volts) supply to prevent damage to the device due to transients causing latch up.

Vdd should be bypassed to digital ground with a high frequency 0.1uF (or larger) capacitor. Analog ground should be bypassed to Vss and all 5 reference resistor taps should be bypassed to analog ground.

The converter is biased by a resistor from Vdd to the BIAS pin. The current in this resistor is approximately 1/100 of the current used by the converter. The bias current is calculated by the formula: (Vsd-Vss -2.0v)/R. For Vdd = 5v, Vss = -5v, and a resistor of 82Kohms, the converter's DC operating current will be approximately 10 mA. Decreasing the resistor towards 47K ohms will increase the operating speed of the converter at the cost of some power. Increased speed may also be provided by using an asymmetric clock. By keeping the RESET time to a minimum of 25 nS one can increase the effective speed of the conversion. Data can be strobed from the device up to 20 nS after the sample time (into the RESET mode). The Vin line should be driven from a low impedance source of 100 ohms or less.

### Device Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>USC1070</th>
<th>USC1071</th>
<th>USC1072</th>
<th>USC1073</th>
<th>USC1170</th>
<th>USC1173</th>
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<tbody>
<tr>
<td></td>
<td>Min</td>
<td>Max</td>
<td>Min</td>
<td>Max</td>
<td>Min</td>
<td>Max</td>
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<tr>
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<td>0</td>
<td>8</td>
<td>0</td>
<td>8</td>
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<tr>
<td>DLE **</td>
<td></td>
<td></td>
<td>(1)</td>
<td>(1)</td>
<td>+/ 40</td>
<td>+/- 40</td>
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<td>Ladder Resistance</td>
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<td>2</td>
<td>6</td>
<td>10</td>
<td>30</td>
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<td>Supply Current (2)</td>
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<td>1</td>
<td>20</td>
<td>0.5</td>
<td>10</td>
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<td>90</td>
<td>300</td>
<td>90</td>
<td>90</td>
<td>90</td>
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<tr>
<td>Number of Pins</td>
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<td>24</td>
<td>24</td>
<td>24</td>
<td>24</td>
<td>24</td>
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</tbody>
</table>

** DLE:Differential Linearity Error; (1) +/- 40 mV for 1 LSB version; +/- 20 mV for 2 LSB version; (2) programmable, excludes ladder current
12 BIT CONVERSION

High speed precision conversions can be attained as shown in Figure 1. A sample/hold (S/H) module is required to sample the incoming signal. The reading is taken in a two step process. With \( \varnothing \) low, the flash converter is connected to the S/H output (Vin). CK1 then goes low and this provides a 7 bit digital output that is stored in a latch when \( \varnothing \) goes high. The output of the latch drives a 7 bit binary adder. Its output, which presently is the same as the latch, is then stored in DAC when CK1 returns high. Note that the converter, reference voltages are 0.1V high. This means that the digital output is typically two counts low.

The output of the DAC (+/-3.2V full scale swing) is added to a 96.9mV offset (100mV-(100/32)mV) which adjusts for the two count error in the first reading and the 0.1V shift in the converter's reference voltage. The composite signal is then subtracted from a differential amplifier with a gain of 32. Its output drives the converter which then digitizes this remaining signal when CK1 goes low again. The lower 5 bits of data appear at the output.

The upper two bits are gated into the adder and summed with the previous 7 most significant bits when CK2 goes high. The 12 bit result is now available at the outputs. This scheme will correct errors in the first approximation that are (up to) two counts off.

As an example, suppose Vin = +0.03V which looks like -0.07V to the converter's input due to the 0.1V offset. This would normally give a reading of 0111111. Assume there is an error and the output is 0111110 (62). The DAC would put out a signal of (62/128) x 6.4 - 3.2 = -0.100V which is offset by 0.0969 to give -0.0031. The x 32 amplifier puts out 32 x (0.03 - (-0.0031)) = +1.059V which looks like +0.959 to the flash converter and becomes digitized as 1001011 (83). The final output is then ((62 + 2) x 32) + 19 = 2067 which represents a signal (2067/4096) x 6.4 - 3.2 = 29.7mV which is very close to the input value of 30mV.

FIGURE 1 : 12 BIT A/D CONVERTER
TYPICAL PIN CONFIGURATIONS

20 PIN

24 PIN

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Universal Semiconductor

MIN / MAX OPERATING VOLTAGES

Ordering Information

The basic structure is USC prefix; 10 for open drain output or 11 for 3-state output; 70 for standard flash, 71 for 12 bit half flash applications, 72 for ultra low power, & 73 for 20 pin plastic; - A for 1/2 LSB accuracy, -B for 1 LSB; I for industrial temperature, M for military temp; -C for cerdip, -P for plastic, & -L for leadless chip carriers; - 24 or -20 for the package pin count. Examples:

USC1070—AM—C24 1/2 LSB Military Temperature
USC1073—BI-P20 1 LSB 20 Pin Industrial
USC1071—AI-DIE 1/2 LSB DIE for 12 BIT

24 LEAD CERDIP

20 LEAD PLASTIC

All dimensions in inches and (millimeters)